AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in this application.

1.(Currently Amended)   A method to correct timing of a phase modulated signal, comprising:

applying a received phase modulated (PM) signal to a first circuit branch and a second circuit branch;

in the first circuit branch, selecting k data bits from the received (PM) signal, wherein a data bit received most recently corresponds to a time t_1 and wherein k is an integer greater ~~than 1~~than 1;

determining a timing weight factor based on the k data bits;

in the second circuit branch, delaying the received PM signal to a second time t_2 that is later than the first time t_1;

adjusting a phase of the delayed PM signal;

applying the timing weight factor to at least a portion of the ~~delayed and~~ phase-adjusted delayed PM signal to calculate a timing offset; and

using the timing offset to correct timing of a PM signal received subsequent to the time t_1.

2.(Original)   The method of claim 1 wherein selecting k data bits comprises arranging the k data bits serially so as to alternate between in-phase and quadrature bits.

3.(Original)   The method of claim 1 further comprising:

setting k equal to a total number of data bits that influence timing of the received PM signal at the first time t_1.

4.(Original)   The method of claim 1 wherein $k=1+\dfrac{1}{BT}$, wherein B is a bandwidth of the received signal and T is a bit interval of the received signal.

5.(Original)   The method of claim 1 wherein determining a timing weight factor includes accessing, using the k data bits, a lookup table that outputs a time derivative of phase.

6.(Original)   The method of claim 5 wherein determining a timing weight factor comprises inverting a sign of a derivative of phase with respect to time when the most recent data bit is one of an in-phase or a quadrature data bit.

7.(Original)   The method of claim 1 wherein determining a timing weight factor comprises correlating the k data bits except the most recent data bit with a derivative with respect to time of a conjugate of a waveform reconstructed from the received PM signal.

8.(Original)   The method of claim 7 wherein the derivative with respect to time is stored in a lookup table.

9.(Currently Amended)   A method to correct timing and phase of a phase modulated (PM) signal, comprising:

applying a received phase modulated (PM) signal to a first circuit branch and a second circuit branch;

in the first circuit branch, selecting k data bits from the received PM signal, wherein a data bit received most recently corresponds to time t_1 and wherein k is an integer greater than 1;

determining a phase correction factor and a timing weight factor based on differentially weighted the k data bits;

apart from the first circuit branch, delaying the received PM signal to a second time t_2 that is later than t_1;

in the second circuit branch, adjusting a phase of the delayed PM signal based on the phase correction factor;

correcting the phase of a PM signal received after time t_1 with a phase offset generated by the phase-adjusted delayed version of the PM signal;

multiplying the delayed, phase–adjusted delayed version of the PM signal with the timing weight factor to determine a timing offset; and

adjusting the timing of the PM signal received after time t_1 with the timing offset.

10.(Currently Amended)   A circuit to correct timing of a received phase modulated (PM) signal, comprising:

a first circuit branch wherein a register, one of an algorithm sub-circuit and a lookup table sub-circuit, and a loop phase shifter are arranged in electrical series, in that order;

a second circuit branch having an input in parallel with the first circuit branch, wherein a delay block and the loop phase shifter are arranged in electrical series, in that order;

a timing adjust block;

the register for storing a series of at least two data bits sampled from a PM signal, the most recent data bit sampled at a first time; and

a multiplier having synchronized inputs coupled to an output of the loop phase shifter and to an output of the one of an-the algorithm sub-circuit and a-the lookup table sub-circuit, said multiplier having an output coupled to an input of the timing adjust block.

11.(Original) The circuit of claim 10 wherein the series of at least two data bits alternates between an in-phase bit and a quadrature bit.

12.(Currently Amended)   The circuit of claim 10 wherein the series of at least two data bits comprises $k=n(1+\frac{1}{BT})$ data bits, wherein n is a number of samples per bit interval that is greater than or equal to one, B is a bandwidth of the received signal and T is a bit interval of the received PM signal.

13.(Currently Amended)   The circuit of claim 10 further comprising an inverter disposed between the multiplier and the one of an-the algorithm sub-circuit and a-the lookup table sub-circuit.

14.(Currently Amended)   The circuit of claim 10 wherein the one of an-the algorithm sub-circuit and a-the lookup table sub-circuit outputs the-a timing weight factor by correlating the series of data bits in the register, except the most recent data bit, with a derivative with respect to time of a conjugate of a reconstructed PM waveform.

15.(Original) The circuit of claim 10 wherein the delay block is disposed between the timing adjust block and the loop phase shifter.

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16.(Currently Amended)   The circuit of claim 10 further comprising a second timing adjust block disposed between the delay block and the ~~second timing adjust block~~ loop phase shifter.

17.(Currently Amended)   A circuit to correct timing and phase of a phase modulated (PM) signal, comprising:

a first circuit branch wherein a register, one of an algorithm sub-circuit and a lookup table sub-circuit, and a loop phase shifter are arranged in electrical series in that order;

a second circuit branch having an input in parallel with the first circuit branch, wherein a delay block and the loop phase shifter are arranged in electrical series in that order;

a timing adjust block;

a primary phase shifter in electrical series with the timing adjust block having an input coupled to an output of the loop phase shifter; and

a multiplier having inputs coupled to an output of the loop phase shifter and to an output of the one of ~~an~~ the algorithm sub-circuit and ~~a~~ the look-up table sub-circuit, and having an output coupled to an input of the timing adjust block.

18.(Currently Amended)   The circuit of claim 17 wherein ~~each of~~ the said inputs to the multiplier ~~and the loop phase shifter defines two inputs that~~ are synchronized.

19.(Original) The circuit of claim 17 wherein the delay block is disposed between the timing adjust block and the loop phase shifter.

20.(Original) The circuit of claim 17 further comprising a second timing adjust block disposed between the delay block and the loop phase shifter.